What is claimed is:

CLAIMS

1. A memory cell having a square feature size of less than $4F^2$ comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel; and

a substantially horizontal floating gate formed over at least a portion of the drain, wherein the feature size of the memory cell is not greater than $2F^2$.

2. The memory cell of claim 1, wherein the source is a buried layer.

3. The memory cell of claim 1, wherein the horizontal floating gate is a sub lithographic floating gate.

4. The memory cell of claim 1, wherein the horizontal floating gate is a sub lithographic floating gate defined by a spacer.

5. The memory cell of claim 1, wherein the horizontal floating gate is a self aligned floating gate.

6. A memory cell having a square feature size of less than $4F^2$ comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel;

a substantially horizontal floating gate formed over at least a portion of the drain; and

a substantially vertical select gate formed substantially perpendicular to the horizontal floating gate in a trench, wherein the select gate is adjacent to the vertical channel.

7. The memory cell of claim 6, wherein the memory cell has a minimum feature size corresponding to the horizontal floating gate and the vertical select gate.

8. The memory cell of claim 6 further comprising a select source and a select drain coupled to the select gate, wherein the select source, the select gate and the select drain form a select transistor.

9. The memory cell of claim 6, wherein the memory cell has a feature size not greater than $2F^2$.

10. A memory cell having a square feature size of less than $4.5F^2$ comprising:

a first transistor comprising a source, a drain and a gate; and

a select transistor coupled to the first transistor, comprising a source, a drain and a gate, wherein the gate of the select transistor is formed substantially perpendicular to the gate of the first transistor.

11. The memory cell of claim 10, wherein the drain of the first transistor has an upper surface and a lower surface and the source of the first transistor has an upper surface and a lower

surface and the upper surface of the source of the first transistor is located below the lower surface the drain of the first transistor.

12. The memory cell of claim 10, wherein the source and drain of the first transistor are shared as the source and drain of the select transistor.

13. A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer;

a p-type layer formed over the first n-type layer; and

a second n-type layer is formed over the p-type layer, wherein the p-type layer forms a substantially vertical channel, wherein the memory device has memory cells having feature size of less than $4F^2$.

14. The memory device of claim 13, wherein the first n-type layer forms a buried source and the second n-type layer forms a drain.

15. A memory device having a square feature size of less than $4F^2$ comprising:

a horizontal first n-type layer formed over a substrate;

a p-type layer formed over the first n-type layer;

a horizontal second n-type layer is formed over the p-type layer;

a horizontal floating gate formed over the substrate; and

a vertical select gate formed over the substrate, wherein the p-type layer forms a vertical channel, the first n-type layer forms a buried source and the second n-type layer forms a drain.

16. The memory device of claim 15, wherein the vertical select gate is formed substantially perpendicular to the horizontal floating gate.

17. A memory device having a square feature size of less than $4F^2$ comprising:

a buried source formed over a substrate;

a vertical channel formed over the buried source; and

a drain formed over the vertical channel, wherein the vertical channel is formed using epitaxial deposition.

18. A memory device having a square feature size of less than $4F^2$ comprising:

A buried source formed over a substrate;

a vertical channel formed over the buried source; and

a drain formed over the vertical channel, wherein the vertical channel is formed using epitaxial deposition.

19. A memory device having a square feature size of less than $4F^2$ comprising:

a buried source formed over a substrate;

a vertical channel formed over the buried source;

a drain formed over the vertical channel;

a floating gate formed over the substrate; and

a select gate formed perpendicular to the floating gate in a trench formed in the substrate, wherein the memory device has a square feature size of less than $4F^2$.

20. A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate;

a p-type layer formed over the first n-type layer;

a second n-type layer formed over the p-type layer;

a floating gate formed over the substrate;

a trench formed in the substrate; and

a select gate formed on a sidewall of the trench.

21. A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate forming a source;

a p-type layer formed over the first n-type layer forming a vertical channel;

a second n-type layer formed over the p-type layer forming a drain;

a tunnel oxide layer formed over the n-type layer;

a first poly layer formed over at least a portion of the tunnel oxide layer;

trenches formed in the substrate; and

a select gate formed on sidewalls of the trenches.

22. A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a buried source formed over the substrate;

a vertical channel formed over the buried source;

a drain formed over the vertical channel;

a tunnel oxide layer formed over the drain;

a self aligned floating gate formed over the tunnel oxide layer;

a trench formed in the substrate;

an active trench formed in the substrate; and

a select gate formed along sidewalls of the active trench area.

23. A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench is formed in the substrate;

a vertical select gate is formed in the select trench;

digitlines are formed over the second n-type layer;

a self aligned floating gate formed over the n-type layer; and

wordlines formed over the substrate and the digitlines.

24. A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench is formed in the substrate;

a vertical select gate is formed in the select trench;

a conductive layer is formed over at least a portion of the second n-type layer;

a first spacer is formed on the tungsten layer;

a tunnel oxide layer formed over at least a portion of the substrate;

a polysilicon layer formed on the tunnel oxide layer; and

an oxide layer formed on the polysilicon layer.

25. The memory device of claim 24, wherein the conductive layer is a tungsten layer.

26. A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer formed over a substrate, forming a source;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer, forming a drain;

a select trench is formed in the substrate;

a select gate is formed substantially vertical in the select trench, wherein the memory device has a feature size substantially less than $4.5F^2$ or not greater than $2F^2$.

27. The memory device of claim 26, further comprising a tunnel oxide layer formed over the substrate.

28. The memory device of claim 27, further comprising digitlines and wordlines formed over the substrate.

29. The memory device of claim 28, wherein the wordlines are above the digitlines.

30. The memory device of claim 29, wherein the wordlines comprise a poly-WSi layer.

31. The memory device of claim 30, wherein the digitlines comprise at least one tungsten layer.

32. The memory device of claim 31, wherein the digitlines are above at least a portion of the drain.

33. The memory device of claim 32 further comprising a spacer formed between the digitlines and the wordlines.

34. The memory device of claim 26, wherein the drain is doped with Boron.

35. The memory device of claim 26, wherein the floating gate comprises tunnel oxide, polysilicon and oxide layers.

36. The memory device of claim 26, wherein the floating gate is self aligned.

37. A method of fabricating a memory device having a square feature size of $2F^2$ comprising:

providing a substrate;

forming a first n-type layer over the substrate;
forming a p-type layer over the first n-type layer;
forming a second n-type layer over the p-type layer;
forming a floating gate over the substrate;
etching a trench in the memory device; and
forming a select gate in the trench.

38. The method of claim 37, wherein forming a first n-type layer over the substrate comprises forming a buried source over the substrate.

39. The method of claim 37, wherein forming a first p-type layer over the first n-type layer comprises forming a first p-type layer over the first n-type layer using epitaxial deposition.

40. The method of claim 37, forming a p-type layer over the first n-type layer comprises forming a vertical channel over the first n-type layer.

41. A method of fabricating a buried source comprising:
providing a wafer having a substrate;
covering a periphery of a wafer using an array mask;
doping source areas with a dopant; and
performing an epitaxial deposition to form a p-type channel, wherein performing an epitaxial deposition to form a p-type channel comprises performing an epitaxial deposition to form a p-type channel to a determined thickness, wherein the thickness determines a channel length.

42. The method of claim 41, wherein doping source areas with a dopant comprises doping source areas with As.

43. The method of claim 41, wherein doping source areas with a dopant comprises doping source areas with Sb.

44. A method of fabricating a memory device having a square feature size of less than $4F^2$ comprising:

providing a wafer having a substrate;

forming a buried source over the substrate;

forming a vertical channel over the buried source;

performing a cell implant;

forming a tunnel oxide layer over the substrate;

forming a first poly layer over the tunnel oxide layer;

forming a nitride layer over the first poly layer;

patterning wordlines into the memory device;

forming STI areas in the memory device;

removing the nitride layer; and

forming an oxide nitride oxide layer over a surface of the memory device.

45. The method of claim 44, wherein forming STI areas in the memory device further comprises etching the nitride layer and etching the first poly layer.

46. The method of claim 44, wherein forming STI areas in the memory device further comprises depositing a STI oxide over the STI areas and filling the STI areas with a field oxide.

47. The method of claim 44, further comprising:

polishing a surface of the memory device using chemical mechanical polishing to make the surface planar.

48. A method of fabricating a memory device having a square feature size of less than $4F^2$ comprising:

providing a wafer having a substrate;

forming a buried source over the substrate;

forming a vertical channel over the buried source;

forming a STI area and a self aligned floating gate;

depositing a BPSG layer over the substrate;

depositing a hardmask layer over the BPSG layer;

patterning active areas to form an active trench;

forming first spacers along sidewalls of the active trench;

forming a drain in the active trench; and

forming a wordline over the drain.

49. The method of claim 48, further comprising performing RTP on the memory device and polishing the surface of the memory device prior to depositing a hardmask layer.

50. The method of claim 48, wherein patterning active areas further comprises etching through the hardmask layer, the BPSG layer, an oxide nitride oxide layer and a first poly layer.

51. The method of claim 49, wherein forming first spacers comprises depositing a first spacer layer and etching the first spacer layer thereby leaving the first spacers along the sidewalls of the active trench.

52. The method of claim 48, further comprising:
forming a TiN layer over the active trench; and
forming a TiSi layer over the active trench.

53. The method of claim 48 further comprising:
performing a RTP on the memory device prior to forming a wordline.

54. The method of claim 48, wherein forming a wordline comprises:
depositing a wordline layer over the active trench;
polishing the wordline layer such that the wordline layer is planar to the hardmask layer; and
removing a portion of the wordline layer such that a lower portion of the wordline layer remains.

55. The method of claim 54, wherein removing a portion of the wordline layer comprises removing substantially half of the wordline layer.

56. The method of claim 48, further comprising depositing a second spacers over the wordline.

57. A method of fabricating a memory device having a square feature size of about $2F^2$ comprising:
forming active areas in a substrate;
forming a floating gate layer over the substrate;
patterning rowlines in the memory device;
forming a removable spacer over the rowlines; and
etching a select trench in the substrate.

58. The method of claim 57 further comprising:

removing the removable spacer;

forming a select transistor oxide layer over the select trench;

forming a second poly layer over the surface of the memory device;

forming a conductive layer over the second poly layer; and

patterning the second poly layer and the conductive layer.

59. The method of claim 58, wherein forming a conductive layer over the second layer comprises forming a WSi_x layer over the second poly layer.

60. The method of claim 58, wherein forming a second poly layer over the surface of the memory device further comprises forming the second poly layer in the select trench to form a select gate.

61. A method of fabricating a memory device having a square feature size of less than $4F^2$ comprising:

forming a source;

forming a drain;

forming a floating gate layer;

forming rowlines;

forming a trench;

forming a select trench; and

forming a select gate.

62. The method of claim 61, wherein forming a source comprises forming a n-type layer over a substrate.

63. The method of claim 61, wherein forming a drain comprises forming a n-type layer over the source.

64. The method of claim 61, wherein forming a floating gate layer comprises:

forming a tunnel oxide layer;

forming a polysilicon layer over the tunnel oxide layer; and

forming an oxide layer over the polysilicon layer.

65. The method of claim 61, wherein forming a select gate comprises:

forming an oxide layer in the select trench; and

filling the select trench with polysilicon.

66. The method of claim 61 further comprising forming digitlines, wherein the digitlines are located above the rowlines.

67. A system comprising:

a plurality of memory devices, wherein at least one of said plurality of memory devices have a square feature size of less than $4F^2$ and comprise:

a source;

a channel formed substantially vertical over the source;

a drain formed over the channel; and

a floating gate formed substantially horizontal over at least a portion of the drain, wherein the feature size of the memory device is substantially less than $4.5F^2$.

68. A computer system comprising:

at least one processor;

a system bus; and

a memory device coupled to the system bus, the memory device including at least one memory cell having a square feature size of less than $4F^2$ and comprising:

a buried source formed in a substrate;

a vertical channel formed over the buried source;

a self aligned floating gate formed over the substrate; and

a select gate in a select trench formed in the substrate.